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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/210,540	12/14/98	NAKAYAMA	H P982413

026263
MM92/0305
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EXAMINER	
KANG, D	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED:
03/05/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)
*U.S. GPO: 2000-473-000/44602

1- File Copy

Office Action Summary	Application No.	Applicant(s)	
	09/210,540	NAKAYAMA, HAJIME	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims **1-5** and **9-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art by applicant in view of Jung (US 5,856,215).

Regarding claim **1**, the admitted prior art by applicant disclosures a semiconductor device comprising (Fig. 2):

a first element formation region in which a device of a first conductivity type is formed; a second element formation region separated from said first element formation region by an element isolation region and in which a device of a second conductivity type different from said first conductivity type is formed; a first gate electrode provided on said first element formation region and containing an impurity of the first conductivity type; a second gate electrode provided on said second element formation region facing said first gate electrode and containing an impurity of the second conductivity type; a first impurity storage region containing said first conductivity type impurity, having one end connected to an end of said first gate electrode; a second impurity storage region containing said first conductivity type impurity, having one end connected to an end of said second gate electrode.

The admitted prior art by applicant does not teach the first and second impurity storage region arranged in a direction different from the direction of arrangement of said first and second gate electrode. Jung teaches the first and second gate electrode has a portion be connected to the end of the first and second electrode arranged in a direction different from the direction of arrangement of the first and second gate electrode. ***See Fig.1***.

It is inherent that the structure taught by Jung will reduce the size of CMOS since the structure is identical to the claimed invention. It is conventional in the art to provide different directions for gate electrodes as taught by Jung in Fig.1. It would have been obvious to one of ordinary skill to change shape of gate electrode in order to achieve high density of CMOS on a wafer.

Regarding claim **2**, the admitted prior art teaches first and second impurity storage regions are physically connected to each other by a semiconductor layer.

Regarding claim **3**, the admitted prior art teaches the other ends of said first and second impurity storage regions are electrically connected to each other through a conductive layer.

Regarding claim **4**, the admitted prior art teaches the first and second impurity storage regions are arranged in a direction perpendicular to the direction of arrangement of said first and second electrodes.

Regarding claim **5**, the admitted prior art teaches the first and second gate electrodes and said first and second impurity storage regions are formed in the same conductive semiconductor layer.

Regarding claim **9**, the admitted prior art teaches semiconductor layer be formed by polycrystalline silicon and first and second gate electrodes and first and second impurity storage regions are formed by selectively implanting impurities to said polycrystalline silicon layer.

Regarding claim **10**, the admitted prior art teaches the width of said semiconductor layer physically connecting said first and second impurity storage regions is a value allowing mask misalignment when forming said first and second gate electrodes and first and second impurity storage regions.

Regarding claim **11**, the admitted prior art teaches the widths of said first and second impurity storage regions are equal to the gate length of said first and second gate electrodes and the lengths of said first and second impurity storage regions are longer than said gate length.

2. Claims **6-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art as modified by Jung as applied to claim 1 as discussed above, and further in view of Joyner et al (US 6,114,741). The teaching of admitted prior art as modified by Jung have been discussed above.

The admitted prior art as modified by Jung does not teach element isolation region be buried in a trench formed a boundary between said first and second conductive type of element formation regions in a semiconductor substrate. However, Joyner et al teaches element isolation region (Fig. 1E) be buried in a trench formed a boundary between said first and second conductive type of element formation regions in a semiconductor substrate in order to isolate first and second conductive type regions.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use trench isolation in order to provide isolation between adjacent device regions.

Regarding claim **7**, Joyner et al teaches element isolation region isolates first and secon element formation region

Regarding claim **8**, Joyner et al teaches element isolation region is buried in a trench formed in semiconductor layers.

Response to Arguments

3. Applicant's arguments filed January 18, 2001 have been fully considered but they are not persuasive.

The applicant argues that Jung fails to discloses first and second impurity regions that are arranged in directions different from first and second gate electrode. Examiner respectfully disagree with that interpretation because Jung clearly teaches in ***Fig.1*** the first and second gate electrode has a portion being connected to the end of the first and second electrode has a portion be connected to the end of the first and second electrode arranged in a direction different from the direction of arrangement of arrangement of the first and second gate electrode.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Donghee Kang** whose telephone number is 703-305-9147. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

DHK
February 27, 2001